IN THE CLAIMS:

Please amend the claims as follows:

1. *(currently amended)* An electrical circuit ~~for providing an electrically operable connection of an external power supply and an electrical device being a motor vehicle built in device,~~ comprising:
   - a main input ~~(P1)~~ for coupling to ~~said~~an external power supply ~~(PS)~~;
   - a main output ~~(P2)~~ for coupling to ~~said~~an electrical device; and
   - a first electrical operable switch ~~(Sw1)~~ interconnected between said main input ~~(P1)~~ and said main output ~~(P2)~~, said first electrical operable switch ~~(Sw1)~~ having an open position and a closed position, said first electrical operable switch ~~(Sw1)~~ being conductive in said closed position and being non-conductive in said open position;

   ~~characterized in that said circuit further comprises:~~
   - at least one wake-up input ~~(I1, I2, I3)~~ to receive a wake-up signal;
   - at least one sleep input ~~(Pd)~~ to receive a sleep signal; and
   - a bi-stable sub-circuit ~~(Crbs)~~ coupled to said main input ~~(P1)~~ and coupled to said first electrical operable switch ~~(Sw1)~~, said sub-circuit ~~(Crbs)~~ being connected to said at least one wake-up input ~~(I1, I2, I3)~~ and to said least one sleep input ~~(Pd)~~ such that

     a received wake-up signal energizes said bi-stable sub-circuit ~~(Crbs)~~ and a received sleep signal de-energizes said bi-stable sub-circuit ~~(Crbs)~~; wherein said energized bi-stable sub-circuit ~~(Crbs)~~ causes said first electrical operable switch ~~(Sw1)~~ to close and said de-energized bi-stable sub-circuit ~~(Crbs)~~ causes said first electrical operable switch ~~(Sw1)~~ to open;

   wherein said bi-stable sub-circuit comprises:
   - a first transistor having an emitter terminal, a collector terminal and a base terminal, wherein said first transistor is configured with a bridge resistor interconnected between its emitter terminal and its base terminal and a base resistor connected to its base terminal;

- a second transistor having an emitter terminal, a collector terminal and a base terminal, wherein said second transistor is configured with a bridge resistor interconnected between its emitter terminal and its base terminal and a base resistor connected to its base terminal; and
- an interposed resistor;

wherein said first transistor is coupled via its emitter terminal to said main input, via its collector terminal to a first terminal of said interposed resistor and via its base resistor to said collector terminal of said second transistor;

wherein said second transistor is coupled via its emitter to ground, via its base resistor to a second terminal of said interposed resistor and via its collector to said base resistor of said first transistor;

wherein said at least one wake-up input is coupled to a first connection line between said base resistor of said first transistor and said collector terminal of said second transistor, both being coupled;

wherein said at least one sleep input is coupled to a second connection line between said base resistor of said second transistor and said second terminal of said interposed resistor, both being coupled; and

wherein said first electrical operable switch is operable with said bi-stable sub-circuit being coupled to said second connection line.

2. *(cancelled)*

3. *(currently amended)* The electrical circuit according to claim ~~2~~1, ~~characterized by~~further comprising:
   - a third transistor ~~(T5)~~ having an emitter terminal, a collector terminal and a base terminal, wherein said third transistor ~~(T5)~~ is configured with a bridge resistor interconnected between its emitter terminal and its base terminal and a base resistor connected to its base terminal;

   wherein said third transistor ~~(T5)~~ is interconnected in-between a connection line coupling said bi-stable sub-circuit ~~(Crbs)~~ and said first electrical operable switch ~~(Sw1)~~ such that said third transistor ~~(T5)~~ is coupled via its base resistor to said

second connection line via its collector terminal to said first electrical operable switch ~~(Sw1)~~ and via its emitter terminal to ground.

4. *(currently amended)* The electrical circuit according to claim ~~2~~1, ~~characterized by~~further comprising:
   - at least one wake-up transistor ~~(T3, T3a, T3b)~~ having an emitter terminal, a collector terminal and a base terminal, wherein said at least one wake-up transistor ~~(T3, T3a, T3b)~~ is configured with a bridge resistor interconnected between its emitter terminal and said its terminal and a base resistor connected to its base terminal;

   wherein said at least one wake-up transistor ~~(T3, T3a, T3b)~~ is interconnected in-between said at least one wake-up input ~~(I1, I2, I3)~~ and said bi-stable cub-circuit ~~(Crbs)~~ such that said at least one wake-up transistor ~~(T3, T3a, T3b)~~ is coupled via its base resistor to said at least one wake-up input ~~(I1, I2, I3)~~, via its emitter terminal to ground and via its collector terminal to said first connection line.

5. *(currently amended)* The electrical circuit according to claim ~~2~~1, ~~characterized by~~further comprising:
   - at least one sleep transistor ~~(T4)~~ having an emitter terminal, a collector terminal and a base terminal, wherein said at least one sleep transistor ~~(T4)~~ is configured with a bridge resistor interconnected between its emitter terminal and its base terminal and a base resistor connected to its base terminal;

   wherein said at least one sleep transistor ~~(T4)~~ is interconnected in-between said at least one sleep input ~~(Pd)~~ and said bi-stable sub-circuit ~~(Crbs)~~ such that said at least one sleep transistor ~~(T4)~~ is coupled via its base resistor to said at least one sleep input ~~(Pd)~~, via its emitter terminal to ground and via its collector terminal to said second connection line.

6. *(currently amended)* The electrical circuit according to claim ~~2~~1, ~~characterized by~~further comprising:
   - an upper voltage level check circuit ~~(Cr1)~~ comprising:
   - a second resistor ~~(R2)~~;

- a z-diode ~~(D1)~~; and
- a fourth transistor ~~(T6)~~ having an emitter terminal, a collector terminal and a base terminal, wherein said fourth transistor ~~(T6)~~ is configured with a bridge resistor interconnected between its emitter terminal and its base terminal and a base resistor connected to its base terminal;

wherein said second resistor ~~(R2)~~ is coupled to a connection line between said main input ~~(P1)~~ and said first electrical operable switch ~~(Sw1)~~ and to a first terminal of said z-diode ~~(D1)~~;

wherein said fourth transistor ~~(T6)~~ is coupled via its base resistor to a second terminal of said z-diode ~~(D1)~~, via its emitter terminal to ground and via its collector terminal to said second connection line; and

wherein said z-diode is adapted to be conductive in case a voltage applied to said main input ~~(P1)~~ exceeds a pre-defined upper voltage level ~~(V_{ZD1})~~.

7. *(currently amended)* The electrical circuit according to claim ~~2~~1, ~~characterized by~~further comprising:
   - a second electrical operable switch ~~(Sw2)~~ interconnected in-between said first electrical operable switch ~~(Sw1)~~ and said main output ~~(P2)~~; and
   - an lower voltage level check circuit ~~(Cr2)~~ comprising
   - a third resistor ~~(R3)~~;
   - a z-diode ~~(D2)~~; and
   - a fifth transistor ~~(T7)~~ having an emitter terminal, a collector terminal and a base terminal, wherein said fifth transistor ~~(T7)~~ is configured with a bridge resistor interconnected between said emitter terminal and said base terminal and a base resistor connected to its base terminal;

   wherein said second resistor ~~(R3)~~ is coupled to a connection line between said first electrical operable switch ~~(Sw1)~~ and said main output ~~(P2)~~ and to a first terminal of said z-diode ~~(D2)~~;

   wherein said fifth transistor ~~(T7)~~ is coupled via its base resistor to a second terminal of said z-diode ~~(D2)~~, via its emitter terminal to ground and via its collector terminal to said second electrical operable switch ~~(Sw2)~~ to be operated; and

wherein said z-diode ~~(D2)~~ is adapted to be conductive in case a voltage applied to said main input ~~(P1)~~ and conducted via said first electrical operable switch ~~(Sw1)~~ being conductive exceeds a pre-defined lower voltage level ~~(V_{ZD2})~~.

8. *(currently amended)* The electrical circuit according to claim 1, ~~characterized in that~~wherein said first electrical operable switch ~~(Sw1)~~ is a metal-oxide field-effect transistor ~~(MOSFET)~~.

9. *(currently amended)* The electrical circuit according to claim 7, ~~characterized in that~~ wherein said second electrical operable switch ~~(Sw1)~~ is a metal-oxide field-effect transistor ~~(MOSFET)~~.

10. *(currently amended)* The electrical circuit according to claim ~~2~~1, ~~characterized by~~further comprising:
    - a third z-diode interconnected between said second terminal of said interposed resistor ~~(R1)~~ and said base terminal of said second transistor ~~(T2)~~ within said second connection line;

    wherein said z-diode is adapted to be conductive in case a voltage applied to said main input ~~(P1)~~ and conducted via said first transistor ~~(T1)~~ being conductive exceeds a pre-defined voltage level.

11. *(currently amended)* The electrical circuit according to claim 1, wherein said ~~motor vehicle built-in~~ electrical device is a free-hand installation main device ~~(200)~~ for detachably connecting a mobile communication device ~~(100)~~ and said external power supply ~~(PS)~~ is a battery of a motor vehicle.

12. *(currently amended)* A motor vehicle built-in device ~~being operably connected to an external power supply,~~ comprising:
    - a plurality of electrical components energized by ~~said~~an external power supply; and
    - an electrical circuit ~~(210)~~ for providing an electrical operable connection of ~~an~~said external power supply and said motor vehicle built-in device,

~~characterized in that~~wherein said electrical circuit ~~(210)~~ comprises:

- a main input ~~(P1)~~ for coupling to said external power supply ~~(PS)~~;
- a main output ~~(P2)~~ for coupling to said motor vehicle built-in device;
- a first electrical operable switch ~~(Sw1)~~ interconnected between said main input ~~(P1)~~ and said main output ~~(P2)~~, said first electrical operable switch ~~(Sw1)~~ having an open position and a closed position, said first electrical operable switch ~~(Sw1)~~ being conductive in said closed position and being non-conductive in said open position;
- at least one wake-up input ~~(I1, I2, I3)~~ to receive a wake-up signal;
- at least one sleep input ~~(Pd)~~ to receive a sleep signal; and
- a bi-stable sub-circuit ~~(Crbs)~~ coupled to said main input ~~(P1)~~ and coupled to said first electrical operable switch ~~(Sw1)~~, said sub-circuit ~~(Crbs)~~ being connected to said at least one wake-up input ~~(I1, I2, I3)~~ and to said least one sleep input ~~(Pd)~~ such that

  a received wake-up signal energizes said bi-stable sub-circuit ~~(Crbs)~~ and a received sleep signal de-energizes said bi-stable sub-circuit ~~(Crbs)~~; wherein said energized bi-stable sub-circuit ~~(Crbs)~~ causes said first electrical operable switch ~~(Sw1)~~ to close and said de-energized bi-stable sub-circuit ~~(Crbs)~~ causes said first electrical operable switch ~~(Sw1)~~ to open;

wherein said bi-stable sub-circuit comprises:

- a first transistor having an emitter terminal, a collector terminal and a base terminal, wherein said first transistor is configured with a bridge resistor interconnected between its emitter terminal and its base terminal and a base resistor connected to its base terminal;
- a second transistor having an emitter terminal, a collector terminal and a base terminal, wherein said second transistor is configured with a bridge resistor interconnected between its emitter terminal and its base terminal and a base resistor connected to its base terminal; and
- an interposed resistor;

wherein said first transistor is coupled via its emitter terminal to said main input, via its collector terminal to a first terminal of said interposed resistor and via its base resistor to said collector terminal of said second transistor;

wherein said second transistor is coupled via its emitter to ground, via its base resistor to a second terminal of said interposed resistor and via its collector to said base resistor of said first transistor;

wherein said at least one wake-up input is coupled to a first connection line between said base resistor of said first transistor and said collector terminal of said second transistor, both being coupled;

wherein said at least one sleep input is coupled to a second connection line between said base resistor of said second transistor and said second terminal of said interposed resistor, both being coupled; and

wherein said first electrical operable switch is operable with said bi-stable sub-circuit being coupled to said second connection line..

13. *(cancelled)*

14. *(currently amended)* The motor vehicle built-in device according to claim 12, ~~characterized in that~~ wherein said motor vehicle built-in device ~~(200)~~ is a free hand installation main device ~~(200)~~ for detachably connecting a mobile communication device ~~(100)~~ and said external power supply is a battery of a motor vehicle.

15. *(currently amended)* The motor vehicle built-in device according to claim 14, further comprising:

- at least one interface for exchanging signals ~~(211, 212, 205)~~ between electrical units included in said motor vehicle and said motor vehicle built-in device ~~(200)~~, said signals ~~(211, 212, 205)~~ comprising said at least one wake-up signal and said at least one sleep signal;
- at least one interface for exchanging a signal ~~(201)~~ between said motor vehicle built-in device ~~(200)~~ and said mobile communication device ~~(100)~~ connected detachably ~~(105)~~; and

at least one control unit to pass signals in-between said interfaces.

16. (new) An electrical circuit comprising:

- means for coupling to an external power supply;
- means for coupling to an electrical device; and
- means for providing a first electrical operable switch interconnected between said means for coupling to an external power supply and said means for coupling to an electrical device, said first electrical operable switch having an open position and a closed position, said first electrical operable switch being conductive in said closed position and being non-conductive in said open position;
- means for receiving a wake-up signal;
- means for receiving a sleep signal; and
- means for providing a bi-stable sub-circuit coupled to said means for coupling to an external power supply and coupled to said first electrical operable switch, said sub-circuit being connected to said means for receiving a wake-up signal and to said means for receiving a sleep signal such that

  a received wake-up signal energizes said bi-stable sub-circuit and a received sleep signal de-energizes said bi-stable sub-circuit; wherein said energized bi-stable sub-circuit causes said first electrical operable switch to close and said de-energized bi-stable sub-circuit causes said first electrical operable switch to open;

wherein said bi-stable sub-circuit comprises:

- a first transistor having an emitter terminal, a collector terminal and a base terminal, wherein said first transistor is configured with a bridge resistor interconnected between its emitter terminal and its base terminal and a base resistor connected to its base terminal;
- a second transistor having an emitter terminal, a collector terminal and a base terminal, wherein said second transistor is configured with a bridge resistor interconnected between its emitter terminal and its base terminal and a base resistor connected to its base terminal; and
- an interposed resistor;

wherein said first transistor is coupled via its emitter terminal to said means for coupling to an external power supply, via its collector terminal to a first terminal of

said interposed resistor and via its base resistor to said collector terminal of said second transistor;

wherein said second transistor is coupled via its emitter to ground, via its base resistor to a second terminal of said interposed resistor and via its collector to said base resistor of said first transistor;

wherein said means for receiving a wake-up signal is coupled to a first connection line between said base resistor of said first transistor and said collector terminal of said second transistor, both being coupled;

wherein said means for receiving a sleep signal is coupled to a second connection line between said base resistor of said second transistor and said second terminal of said interposed resistor, both being coupled; and

wherein said first electrical operable switch is operable with said bi-stable sub-circuit being coupled to said second connection line.